AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit (IC), including circuitry arranged in an array having a plurality of rows and a plurality of columns, wherein each row of the plurality of rows begins at a first side of the IC and ends at a second side of the IC, and each column of the plurality of columns begins at a third side of the IC and ends at a fourth side of the IC, the IC comprising:

a column of the plurality of columns comprising a plurality of circuit elements of a circuit type substantially occupying the column; and

a row of the plurality of rows positioned at the third side of the IC, wherein a number of circuit elements of an input and output circuit type in the row is less than a number of remaining circuit elements of other circuit types in the row ; and

wherein there does not exist a perimeter input/output (I/O) ring.

2. (Original) The integrated circuit of claim 1 wherein the circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit type, an Input/Output Block (IOB) type, and an application specific circuit type.

3. (Original) The integrated circuit of claim 1 wherein the input and output circuit type is an Input/Output Block (IOB) type.

4. (Original) The integrated circuit of claim 1 wherein the input and output circuit type includes an Input/Output Block type and a Multi-Giga Bit Transceiver type.

5. (Original) The integrated circuit of claim 1 further comprising a center column comprising configuration logic.

6. (Original) The integrated circuit of claim 3 wherein the center column is positioned on or near the center axis of the IC.

7. (Original) The integrated circuit of claim 4 further comprising a clock column adjacent to the center column.

8. (Original) The integrated circuit of claim 1 wherein the column of the plurality of columns further comprises a spacer tile and a clock tile.

9. (Original) The integrated circuit of claim 1 further comprising an embedded processor.

10. (Currently Amended) An integrated circuit (IC) comprising circuitry having programmable functions and programmable interconnects, the IC further comprising:

a plurality of homogeneous columns and

wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC, and

wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column, and

wherein when the circuit elements of the first set comprise logic blocks there is no input/output block between the end of the first column and the side of the IC.

11. (Original) The integrated circuit of claim 10:

wherein a second column of the plurality of homogeneous columns comprises a second set of substantially identical circuit elements of a second circuit type substantially filling the second column, and

wherein a third column of the plurality of homogeneous columns comprises a third set of substantially identical circuit elements of a third circuit type substantially filling the third column.

12. (Original) The integrated circuit of claim 10 further comprising a heterogeneous center column having configuration logic, a clock management circuit element.

13. (Original) The integrated circuit of claim 10 wherein the first circuit type is selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a fixed logic type, an Input/Output Interconnect (IOI) circuit type, and an Input/Output Block (IOB) type.

14. (Original) The integrated circuit of claim 13 wherein the fixed logic type comprises a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, and an application specific circuit type.

15. (Original) The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a field programmable gate array (FPGA).

16. (Original) The integrated circuit (IC) of claim 10 wherein the integrated circuit further comprises a programmable logic device (PLD).

Claims 17-23 (Cancelled)

24. (Currently Amended) An integrated circuit (IC) comprising:

a plurality of columns and

wherein each of the columns starts at one side of the IC and ends at an opposite side of the IC,

wherein a first column of the plurality of columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column,

wherein when the first circuit type comprises logic blocks, the first column does not have an input/output block at an end of the first column, and

wherein a second column of the plurality of columns comprises a second set

of substantially identical circuit elements of a second circuit type substantially filling the second column~~, and~~

~~wherein a third column of the plurality of columns comprises a third set of substantially identical circuit elements of a third circuit type substantially filling the third column~~.

25. (Original) The integrated circuit of claim 24 further comprising circuitry having programmable functions and programmable interconnects.

26. (Original) The integrated circuit of claim 25 wherein the first, and second, [[and third]] circuit types have a circuit type selected from a group consisting of a Configurable Logic Block (CLB) type, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory (BRAM) type, a Digital Signal Processor (DSP) circuit type, a multiplier circuit type, an arithmetic circuit type, an Input/Output Interconnect (IOI) circuit type, an Input/Output Block (IOB) type, and an application specific circuit type.

27. (Original) The integrated circuit of claim 26 further comprising a heterogeneous center column having configuration logic, a clock management circuit element, and an input/output block.

28. (Original) The integrated circuit of claim 24 wherein the substantially identical circuit elements are substantially identical tiles.

29. (Original) The integrated circuit of claim 28 wherein each tile comprises a functional element coupled to a switch matrix.

Claims 30-33 are cancelled.

34. (New) An integrated circuit (IC) comprising circuitry having programmable functions and programmable interconnects, the IC further comprising:

a heterogeneous center column having configuration logic, a clock

management circuit element, and an input/output block;

a plurality of homogeneous columns and

wherein each of the homogeneous columns starts at one side of the IC and ends at an opposite side of the IC, and

wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type substantially filling the first column.